REMARKS

Claims 5-10, 18-21, 23-32, 36-42 are all the claims pending in the application. This Amendment amends claims 29, 36, 37, 40, and addresses each point of rejection raised by the Examiner. Favorable reconsideration is respectfully requested.

Applicants thank the Examiner for the indication that claims 40-42 are allowed, and for the courtesy extended by the Examiner and SPE Beausoliel to Applicants' undersigned representative at the personal interview conducted August 24, 2005.

With regard to the personal interview, the Form PTOL-413 provided by the Examiner is a complete and accurate record, with the exception of the date: the Form indicates the date of interview as 23 August, 2005, whereas the interview occurred on 24 August, 2005.

At the interview, the exhibits discussed were U.S. Patent 6,480,923 and several excerpts from PCI-Standard documents. All documents that were discussed are specifically identified below, and if not already of record, are submitted herewith. The arguments presented at the interview are memorialized below, as is a discussion of the agreement reached to amend claim 29 made at the interview.

As an editorial matter, Applicants amend claim 36 to change "when" to "if"; amend claim 37 to clarify the relationship between the data request *on the external bus* and the harassing transaction; and amend claim 40 to correct punctuation. These changes are intended to improve form, and are not in response to the Examiner's rejections. These changes were brought to the Examiner's attention at the interview.

Claims 29-32 and 36 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,480,923 to Moertl *et al.* ("Moertl"). All five claims are rejected based entirely upon the passage at column 3, lines 4-9 of Moertl, which reads:

> PCI ordering rules require that read transactions "push" previous write transactions ahead of them. In the case of delayed transactions for PCI, the master that initiates the request must get back on the bus and repeat the original request again and again until the transaction completes.

This passage of Moertl is clearly referring to the ordering rules of the PCI Standard. To clarify the record, Applicants submit herewith copies of the following portions of the PCI Standard from the same time period as Moertl:

- Chapter 3 entitled "Bus Operation" of the *PCI Local Bus Specification*, Production Version, Revision 2.2, December 18, 1998 (pages 21-112).
- Appendix E entitled "System Transaction Ordering" of the *PCI Local Bus Specification*, Revision 2.2, December 18, 1998 (pages 267-278).
- Chapter 5 entitled "Buffer Management" of the *PCI-to-PCI Bridge Architecture Specification,* Revision 1.1, December 18, 1998 (pages 69-92).

Moertl should be interpreted as it would be generally understood in the art. Notably, the *PCI Local Bus Specification* is explicitly incorporated by reference in Moertl. (*Moert,* col. 6, lines 5-10). Further, while Moertl discloses a different buffering scheme than conventional PCI bridges (*see, e.g.,* Moertl col. 7, lines 6-25), the *PCI-to-PCI Bridge Architecture Specification* is relevant at least for its explanation of the protocol environment in which the bridges operate.

Based on these materials, Applicants respectfully submit that the Examiner's "interpretations" are inconsistent with what is generally understood about PCI ordering rules in the art, and that the PCI ordering rules referred to by Moertl do not anticipate the rejected claims.

As illustrative of the PCI ordering rules that Moertl is discussing, Applicants present the following excerpts, which were discussed at the interview, from the PCI specifications for the Examiner's consideration:

> "One performance optimization that PCI systems are allowed to do is the posting of memory write transactions. Posting means the transaction is captured by an intermediate agent; e.g., a bridge from one bus to another, so that the transaction completes at the source before it actually completes at the intended destination. ... While posting improves system performance, it complicates event ordering." (*Bus Spec. App. E,* p. 267).
>
> "The order of a transaction is determined when it completes. Transactions terminated with Retry are only requests and can be handled by the system in any order." (*Bus Spec. App. E,* p. 269) "Retry refers to [a target-initiated] termination requested before any data is transferred because the target is busy and temporarily unable to process the transaction." (*Bus Spec. Ch. 3,* p. 52). "The target signals

Retry by asserting STOP#[1] and not asserting TRDY# on the initial data phase of the transaction... When the target uses Retry, no data is transferred." (*Id.*).

"Memory writes can be posted in both directions in a bridge. ... Read transactions (Memory, I/O, or Configuration) are not posted. ... A read transaction must push ahead of it through the bridge any posted writes originating on the *same* side of the bridge and posted *before* the read. Before the read transaction can complete on its originating bus, it must pull out of the bridge any posted writes that originated on the *opposite* side and were posted *before* the read command completes on the read-destination bus." (*Bus Spec. App. E.*, p. 270; *see also Bridge Spec. Ch. 5*, p. 78 and 82-83).

"A target that uses Delayed Transactions may be designed to have any number of Delayed Transactions outstanding at one time. Only non-posted transactions can be handled as Delayed Transactions. A master must repeat any transaction terminated with Retry since the target may be using a Delayed Transaction. Once a Delayed Request has been attempted on the destination bus, it must continue to be repeated until it completes on the destination bus. Before it is attempted on the destination bus, it is only a request and may be discarded at anytime." (*Bridge Spec. Ch. 5*, p. 78-29).

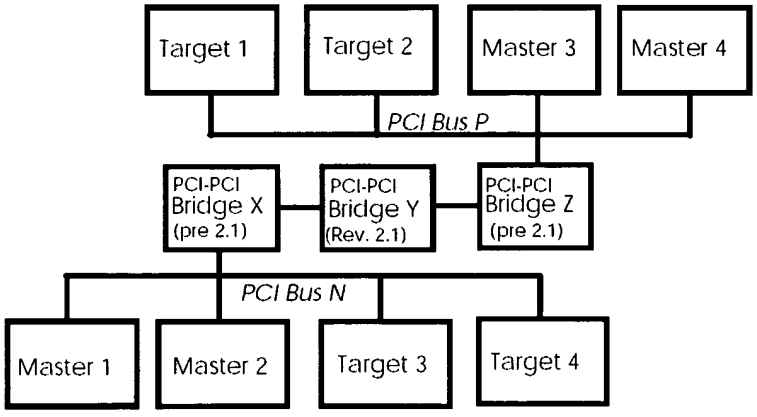

Figure 5-1: Example System with PCI-to-PCI Bridges

(Figure 5-1 from p. 84 of *Bridge Spec. Ch. 5*).

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[1] STOP# and TRDY# are bus signal lines. *See, for example, Bus Spec, Ch. 3*, Section 3.3.3.2.1.

"A Delayed Transaction progresses to completion in three phases:

1. Request by the master

2. Completion of the request by the target

3. Completion of the transaction by the master

During the first phase, the master generates a transaction on the bus, the target decodes the access, latches the information required to complete the access, and terminates the request with Retry. The latched request information is referred to as a Delayed Request. During the second phase, the target independently completes the request on the destination by using the latched information from the Delayed Request. The result of completing the Delayed Request on the destination bus produces a Delayed Completion, which consists of the latched information of the Delayed Request and the completion status (and data if a read request). During the third phase, the master successfully rearbitrates for the bus and reissues the original request. The target decodes the request and gives the master the completion status (and data if a read request). At this point, the Delayed Completion is retired and the transaction has completed." (*Bus Spec. App. E*, p. 272; *see also* Moertl col. 6, lines 20-44).

Referring to the rejection of **claim 29**, a delayed PCI request does not result in "detecting an onset of a first transaction on an external bus" and "issuing a read request in a second transaction on the external bus, the read request directed to the same address as the first transaction.

Applicants understood the Examiner to be asserting that a repeating of the read request by the master constitutes the second transaction. However, the master repeats the read request in response to the Retry instruction from the target -- not in response to detecting an onset of the first transaction on the external bus.

Further, if the "target" is the destination, the target sends the master a Retry, which is not "the read request directed to the same address as the first transaction." Later, when the target completes the transaction, the data in response to the read request is sent to the master, but that also is not "the read request directed to the same address as the first transaction." This is also the

case if an inbound Delayed Request transaction is buffered in a PCI-to-PCI router. *See, e.g.,* Moertl col. 6, lines 55-67. Additionally, if a router were to buffer an outbound read request before relaying it to its target destination, the second transaction is on a different bus (the destination bus) than the first transaction.

Accordingly, Applicants' representative submitted at the interview that **claim 29** is not anticipated, and that **claims 30-32** are also not anticipated, at least as further limitations on **claim 29**.

While there was general agreement in principle with regard to claim 29, the Examiner expressed concern that the relationship between the steps was not entirely clear. Specifically, the Examiner pointed out that the claim recitation of "the *same* address as the first transaction" did not specifically require that the "same" address actually be the address that was acquired by reading from the bus, giving rise to the scenario underlying the rejection in which the address used by a master on retry is a *same* address, albeit not an address acquired by a read from the bus. To resolve this concern, agreement was reached at the interview to amend claim 29 to read "the read request directed to the ~~same~~ address read from ~~as the~~ said first transaction from the external bus."

Referring to the rejection of **claim 36**, a delayed PCI request does not result in "storing a request type in a register" and "when [*or* 'if' as amended] the request type of the [transaction observed on the external bus] matches the request type stored in the register, generating a data request on the external bus."

Applicants understood the Examiner to equate the repeating of the read request by the master with the limitations of the claim. However, as discussed above with **claim 29**, the master repeats the request in response to a Retry -- not based on whether the request type matches a type stored in a register. Likewise, Delayed Request buffering does not result in a data request being generated on the external bus on which the transaction was observed.

At the interview, agreement was reached that claim **36** is not anticipated and overcame the prior of record.

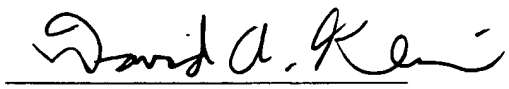
Allowance of claims 29-32 and 36 is requested.

Applicants authorize the Commissioner to charge any fees determined to be due with the exception of the issue fee and to credit any overpayment to Deposit Account No. 11-0600.

The Examiner is invited to contact the undersigned at (202) 220-4209 to discuss any matter concerning this application.

Respectfully submitted,
KENYON & KENYON

Dated: September 2, 2005



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